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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,074	08/04/2003	James M. Wark	2948.7US (96-0555.06/US)	5248

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EXAMINER	
LEBENTRITT, MICHAEL	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,074	WARK, JAMES M.	
	Examiner	Art Unit	
	Michael S. Lebentritt	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 08/04/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 8/4/2003 was filed before the mailing date of the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner is considering the information disclosure statement.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-31 of U.S. Patent No. 6,605,489. Although the conflicting claims are not identical, they are not patentably distinct from each other because similar subject matter is claimed:

connecting at least one pad of the first plurality of (flip chip) (flip chip) pads to at least one pad of the second plurality of (wire bond) (flip chip) pads; providing a first integrated circuit die having a front-side surface having a plurality of flip-chip bumps thereon and having a back-side surface; positioning the front-side surface of the first

integrated circuit die facing the surface of the base; aligning at least one flip-chip bump of the plurality of flip-chip bumps on the front-side surface of the first integrated circuit die with at least one pad of the first plurality of (flip chip) (flip chip) pads on the surface of the base; connecting the at least one flip-chip bump of the plurality of flip-chip bumps on the front-side surface of the first integrated circuit die to the at least one pad of the first plurality of (flip chip) pads on the surface of the base; providing a second integrated circuit die having a front-side surface having a plurality of bond (flip chip) pads thereon and having a back-side surface; positioning the back-side surface of the second integrated circuit die facing the back-side surface of the first integrated circuit die; attaching the back-side surface of the second integrated circuit die to the back-side surface of the first integrated circuit die; connecting at least one bond pad of the plurality of bond (wire bond) pads on the front-side surface of the second integrated circuit die to at least one pad of the second plurality of (wire bond) pads on the surface of the base; and sealing between at least a portion of the front-side surface of the first integrated circuit die and the surface of the base.

2. The method of claim 1, further comprising: sealing completely between the front-side surface of the first integrated circuit die and the surface of the base.

3. The method of claim 2, wherein the step of sealing between at least a portion the front-side surface of the first integrated circuit die and the surface of the base comprises underfilling therebetween.

4. The method of claim 1, further comprising: sealing the first integrated circuit die and the second integrated circuit die.

5. The method of claim 4, wherein the step of sealing the first integrated circuit die and the second integrated circuit die comprises: encapsulating the first integrated circuit die and the second integrated circuit die.

6. The method of claim 1, wherein the first plurality of (flip chip)pads on the base and the second plurality of (wire bond) pads on the base are provided by one of screen printing and selectively plating the first plurality of (flip chip) pads and the second plurality of (wire bond) pads on the surface of the base.

7. The method of claim 1, wherein the steps of positioning the first integrated circuit die and positioning the second integrated circuit die comprise: picking and placing the first integrated circuit die and the second integrated circuit die.

8. The method of claim 1, wherein the step of connecting the at least one flip-chip bump of the plurality of flip-chip bumps on the first integrated circuit die to the at least one pad of the first plurality of (flip chip) pads on the base comprises: reflow-soldering the at least one flip-chip bump of the plurality of flip-chip bumps on the first integrated circuit die to the at least one pad of the first plurality of (flip chip) pads on the base.

9. The method of claim 1, further comprising: testing the connection of the at least one flip-chip bump of the plurality of flip-chip bumps on the first integrated circuit die to the at least one pad of the first plurality of (flip chip) pads on the base; determining if the connection is defective; and repairing the connection when defective.

10. The method of claim 1, wherein the step of attaching the back-side surface of the second integrated circuit die to the back-side surface of the first integrated circuit die comprises: attaching the back-side surface of the first integrated circuit die to the back-side surface of the second integrated circuit die using an uncured epoxy; and curing the uncured epoxy.

11. The method of claim 1, wherein the step of connecting the at least one bond pad of the plurality of bond (wire bond) pads on the second integrated circuit die to the at least one pad of the second plurality of (wire bond) pads on the base comprises: wire-bonding the at least one bond pad of the second plurality of bond (wire bond) pads on the second integrated circuit die to the at least one pad of the second plurality of (wire bond) pads on the base.

12. The method of claim 1, further comprising: testing the connection of the at least one bond pad of the plurality of bond (wire bond) pads on the second integrated circuit die to the at least one pad of the second plurality of (wire bond) pads on the base; determining if the connection is defective; and repairing the connection when defective.

13. A method of repairing a flip-chip die connected to a surface of a base having a first plurality of (flip chip) pads

and a second plurality of (wire bond) pads on a surface thereof, the flip-chip die having a front-side surface and back-side surface, the front-side surface having at least one flip-chip bump of a plurality of flip-chip bumps thereon bonded to at least one pad of the first plurality of (flip chip) pads on the surface of the base, at least one pad of the first plurality of (flip chip) pads and at least one pad of the second plurality of (wire bond) pads on the surface of the base each connected to at least one conductor of a plurality of conductors for communication between the flip-chip die and circuitry external to the flip-chip die, said method comprising: attaching a replacement integrated circuit die having a front-side surface and back-side surface to the back-side surface of the flip-chip die, the front-side surface of the replacement integrated circuit die having a plurality of bond (wire bond) pads thereon; stopping communication between the flip-chip die and said external circuitry connected thereto by disconnecting at least one of the first plurality of (flip chip) pads on the surface of the base from the at least one of the plurality of conductors at locations proximal to the (flip chip) pads; electrically connecting at least one bond pad of the plurality of bond (wire bond) pads on the front-side surface of the replacement integrated circuit die to at least one pad of the second plurality of (wire bond) pads on the surface of the base for communication between the replacement integrated circuit die and circuitry external to the replacement integrated circuit die.

14. The method of claim 13, wherein the second plurality of (wire bond) pads on the surface of the base includes at least one pad of the second plurality of (wire bond) pads on the surface of the base is connected to the at least one pad of the first plurality (flip chip) pads of the base.

15. The method of claim 13, wherein stopping communication between the flip-chip die and the external circuitry comprises: disconnecting each pad of the first plurality of (flip chip) pads on the surface of the base from the plurality of conductors at locations proximal to the (flip chip) pads.

16. A method of assembling a multi-chip structure on a base having a surface comprising: forming a first plurality of (flip chip) pads on the surface of the base; forming a second plurality of (wire bond) pads on the surface of the base; interconnecting at least one pad of the second plurality of (wire bond) pads and at least one pad of the first plurality of (flip chip) pads; positioning a first integrated circuit die having a front-side

surface having a plurality of flip-chip bumps thereon and having a back-side surface, the front-side surface of the first integrated circuit die facing the surface of the base, at least one flip-chip bump of the plurality of flip-chip bumps on the front-side surface aligned with at least one pad of the first plurality of (flip chip) pads on the surface of the base; connecting the at least one flip-chip bump of the plurality of flip-chip bumps on the front-side surface of the first integrated circuit die to the at least one pad of the first plurality of (flip chip) pads on the surface of the base; positioning a second integrated circuit die having a front-side surface having a plurality of bond (wire bond) pads thereon and having a back-side surface, the back-side surface of the second integrated circuit die facing the back-side surface of the first integrated circuit die; attaching the back-side surface of the second integrated circuit die to the back-side surface of the first integrated circuit die; connecting at least one bond pad of the plurality of bond (wire bond) pads on the front-side surface of the second integrated circuit die to at least one of the second plurality of (flip chip) pads on the surface of the base; and sealing at least a portion of the gap between the front-side surface of the first integrated circuit die and the surface of the base.

17. The method of claim 16, further comprising: sealing the entire gap between the front-side surface of the first integrated circuit die and the surface of the base.

18. The method of claim 17, wherein the step of sealing the gap between the front-side surface of the first integrated circuit die and the surface of the base comprises: underfilling the gap.

19. The method of claim 16, further comprising: sealing the first integrated circuit die and the second integrated circuit die.

20. The method of claim 19, wherein the step of sealing the first integrated circuit die and the second integrated circuit die comprises: encapsulating the first integrated circuit die and the second integrated circuit die.

21. The method of claim 16, wherein the steps of forming the first plurality of (flip chip) pads and forming the second plurality of (flip chip) pads comprise one of screen printing and selectively plating the first plurality of (flip chip) pads and

the second plurality of (wire bond) pads on the surface of the base.

22. The method of claim 16, wherein the steps of positioning the first integrated circuit die and positioning the second integrated circuit die comprise: picking and placing the first integrated circuit die and the second integrated circuit die.

23. The method of claim 16, wherein the step of connecting the at least one flip-chip bump of the plurality of flip-chip bumps on the first integrated circuit die to the at least one pad of the first plurality of (wire bond) pads on the base comprises reflow-soldering the at least one flip-chip bump of the plurality of flip-chip bumps on the first integrated circuit die to the at least one pad of the first plurality of (wire bond) pads on the base.

24. The method of claim 16, further comprising: testing the connection of the at least one flip-chip bump of the plurality of flip-chip bumps on the first integrated circuit die to the at least one pad of the first plurality of (flip chip) pads on the base; determining if the connection is defective; and repairing the connection when the connection is defective.

25. The method of claim 16, wherein the step of attaching the back-side surface of the second integrated circuit die to the back-side surface of the first integrated circuit die comprises: attaching the back-side surface of the first integrated circuit die and the back-side surface of the second integrated circuit die using uncured epoxy; and curing the uncured epoxy.

26. The method of claim 16, wherein the step of connecting the at least one bond pad of the plurality of bond (flip chip) pads on the second integrated circuit die to the at least one pad of the second plurality of (flip chip) pads on the base comprises: wire-bonding the at least one bond pad of the plurality of bond (flip chip) pads on the second integrated circuit die to the at least one pad of the second plurality of (flip chip) pads on the base.

27. The method of claim 16, further comprising: testing the connection of the at least one bond pad of the plurality of bond (flip chip) pads on the second integrated circuit die to the at least one pad of the second plurality of (flip chip) pads on the base; determining if the connection is defective; and repairing the connection when the connection is defective.

28. A method of repairing a flip-chip die connected to a surface of a die-carrying base, said method comprising: providing a flip-chip die having a front-side surface and a back-side surface, the front-side surface having flip-chip bumps thereon; providing a base having a surface having a first plurality of (flip chip) pads thereon, the first plurality of (flip chip) pads connected to a plurality of conductors for communication between the flip-chip die and circuitry external to the flip-chip die; bonding the front-side surface having flip-chip bumps thereon of the flip-chip die to the first plurality of (flip chip) pads on the surface of the base; forming a second plurality of (wire bond) pads on the surface of the base, at least one pad of the second plurality of (wire bond) pads connected to at least one conductor of the plurality of conductors; bonding a replacement integrated circuit die having an opposing front-side surface having a plurality of bond (wire bond) pads thereon and back-side surface to the back-side surface of the flip-chip die; interrupting communication between the flip-chip die and the external circuitry by disconnecting at least one pad of the first plurality of (flip chip) pads on the surface of the base from at least one conductor of the plurality of conductors by cutting the at least one conductor of the plurality of conductors adjacent the at least one pad of the first plurality of (flip chip) pads; and bonding at least one bond pad of the plurality of bond (wire bond) pads on the front-side surface of the replacement integrated circuit die to the at least one pad of the second plurality of (flip chip) pads on the surface of the base for communication between the replacement integrated circuit die and the external circuitry.

29. The method of claim 28, wherein the step of forming the second plurality of (wire bond) pads includes connecting at least one pad of the second plurality of (wire bond) pads with at least one pad of the first plurality of (flip chip) pads.

30. The method of claim 28, wherein the step of interrupting communication between the flip-chip die and the external circuitry comprises: disconnecting each pad of the first plurality of (flip chip) pads on the surface of the base from each conductor of the plurality of conductors by cutting the at least one conductor of the plurality of conductors adjacent the at least one pad of the first plurality of (flip chip) pads.

31. A method of making a base having a first plurality of (flip chip) pads on a surface thereof, at least one pad of the first plurality of (flip chip) pads connected to at least one

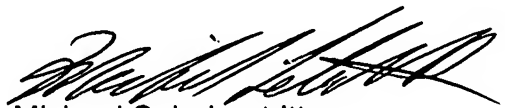
flip-chip bump of a plurality of flip-chip bumps on a first die to be located on the surface of the base, the base used to carry a plurality of integrated circuit dice, the method comprising: forming a second plurality of (flip chip) pads on the surface of the base so at least one pad of the second plurality of (wire bond) pads; connecting each bond pad of a plurality of bond (flip chip) pads on a second die to be located on the first die; and interconnecting each pad of the second plurality of (wire bond) pads on the base and each pad of the first plurality of (flip chip) pads on the base.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. Lebentritt whose telephone number is 571-272-1873. The examiner can normally be reached on 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Michael S. Lebentritt
Primary Examiner
Art Unit 2824

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